* 1/25/18
* Ch14 Processor Structure and Function
* Processor Organization
  + Requirements
    - Fetch instruction - read from memory
    - Interpret instruction - decode instruction
    - Fetch data - read data needed for instruction from memory
    - Process Data - execute instruction
    - Write Data - write data to memory or I/O
    - To do these things, need to store data temporarily, so needs small internal memory
      * Registers
* 1/30/18
* Computer
  + System Bus
    - Address bus
    - Data bus
    - Control bus
  + Memory
  + I/O
  + CPU
    - Internal Bus
    - Registers
      * MAR
      * MBR
      * IOAR
      * IOBR
      * Instruction Register?
      * Program counter?
    - Control unit
    - ALU
      * Status flags
      * Shifter
      * Complementer
      * Arithmetic and Boolean Logic
* User-Visible Registers
  + Categories
    - General purpose
    - Data
      * Hold data, no calculation
    - Address
      * Segment pointers, index register, stack pointer
    - Condition Codes
      * Flags
      * Set by processor hardware as result to operations
* Condition Codes
  + Advantages
    - Reduce number of compare and test instructions needed
    - Conditional instructions are simplified
    - Facilitate branches
    - Condition codes can be saved on the stack
  + Disadvantages
    - Add complexity to hardware and software
    - Modified in different ways by different instructions
      * More difficult for programmer and compiler writer
    - Irregular, require extra hardware connections
    - Must add non-condition-code instructions for special situations (loops)
    - In pipelined implementation, condition codes require special synchronization to avoid conflicts
* Control and status registers
  + Program counter
    - Address of instruction to be fetched
  + Instruction register
    - Instruction most recently fetched
  + Memory address register
  + Memory buffer register
* Program status words (flags)
  + Sign
  + Zero
  + Carry
  + Equal
  + Overflow
  + Interrupt enable/disable
  + Supervisor??? Gates doesn’t know
    - CPU in Supervisor or user mode
* 2/20/18 ---anything after this isn’t on final
* On final project, need to beat 2 warriors(3 for bonus)
* Input/Output
  + Busses
    - System Bus
      * Address Lines
      * Data LInes
      * Control LInes
  + I/O Moddule